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501.35437CV2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: YOSHIDA et al.

Serial No.: 09/416,959

Filed: October 13, 1999

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND PROCESS FOR MANUFACTURING THE SAME

Group: 2812

Examiner: R. Pompey

SUPPLEMENTAL AMENDMENT

Assistant Commissioner
for Patents
Washington, D.C. 20231

October 2, 2002

Sir:

In supplement to the Amendment filed September 3, 2002, please further amend the above-identified application as follows:

In the Claims:

Please amend claims 42 and 47 as follows:

42. (Amended) A semiconductor integrated circuit device having a first portion for a memory array and a second portion for a circuit other than the memory array on a semiconductor substrate comprising:

a MISFET arranged in said first portion, said MISFET having first semiconductor regions and a gate electrode between said first semiconductor regions;

second semiconductor regions arranged in said second portion;

a first insulating film formed over said semiconductor substrate to cover said